Morgan Prior

Design Engineer

Dunbar, EH42 1XD

morgan.prior@gmail.com

SUMMARY

A seasoned engineer with a career spanning roles at Cirrus Logic, Dialog, and Wolfson, contributing to over 20 product tape-outs. My journey in electronics, which began with a passion for high-fidelity audio, has evolved into a focus on CPU/ALU processor design and architecture. I have a proven track record of optimizing designs for power and cost efficiency. My technical competencies include Verilog RTL implementation, Matlab/Simulink modeling, and proficiency in Ruby, with a current focus on developing my Python skills. My commitment to effective communication is demonstrated through my active participation in Toastmasters, which has enhanced my ability to deliver technical training.

EXPERIENCE

Arm, Manchester — *Design Engineer*

November 2025 - PRESENT

Cirrus Logic, Edinburgh — *Design Engineer*

November 2015 - November 2025

Summary: An experienced engineer with a strong history of bringing complex projects to production, evidenced by involvement in 11 tape-outs. Extensive experience in consultation on architectural design, signal processing, and product optimization.

Key Achievements:

- **Pro-Audio Product Line Development:** Directed the DAC architecture for a new pro-audio line, achieving high-fidelity performance at a disruptive price point. Simplified integration for design teams by optimising filter structures to reduce power and enhance jitter robustness.
- **Continuous Glucose Monitor (CGM) Micro-ALU Design:** Architected and programmed a micro-ALU for an innovative continuous glucose monitor product, with a critical focus on achieving aggressive area and power targets essential for this market segment.
- **Enabled Imaging Product Line Relaunch:** Designed and implemented a key Spread Spectrum Clock Generation (SSCG) module, which was a critical component for the successful relaunch of the company's imaging product line.
- **Technical Forum Leadership:** Established and led a monthly signal processing forum fostering knowledge sharing across design groups. Regularly presented on critical technology aspects and facilitated discussions on design challenges and best practices.
- **Advanced Leadership & Communication Skills:** Actively developed public speaking and leadership abilities within Toastmasters International, frequently serving as the lead 'Toastmaster' to host and direct meetings
- **Developed DSP Methodologies:** Authored influential internal articles on advanced DSP techniques, including filter design for cascaded

SKILLS

System-Verilog, Ruby, Python, Shell scripting, Matlab, Claude, Codex, Simulink, Filter design, Micro-ALU design, Git, Subversion, Perforce, Training & Mentoring.

PATENTS

Delay Locked Loops
12438690 (2025)

Class D Amplifier Circuitry
GB2614123 (2024)

Load Detection
US 11.206.487 B2 (2021)

Systems, apparatus and methods for dynamic range enhancement
US 11070183 B1 (2021)

Audio Signal Processing
GB2561757 (2020)

all-pass filters, Wave Digital Filter implementations, and spectral analysis with window normalisation.

Dialog Semiconductors, Edinburgh — *Design Engineer*

July 2011 - October 2015

Summary: Senior member of teams delivering audio and power management projects to production, evidenced by 5 product tape-outs, and 2 test chip tape-outs. Roles included driving requirements, matlab/simulink modelling and RTL implementation.

Key Achievements:

- **Innovated and deployed essential IP blocks** for diverse audio products, such as a high-performance noise gate and limiter for Class-D amplifiers and Dialogs first accessory detection system for TRRS 4-pole headphones.
- **Lead research projects including** Automated filter design methodologies with Mathworks HDL Coder. Resolving Inter-Symbol Interference (ISI) and mismatch errors in current-steering DACs.
- **Managed end-to-end development of next-generation codec filters**, encompassing: MATLAB-based modeling and optimization for performance and cost, including silicon area and clock cycle considerations. Precise fixed-point Simulink modeling for quantization effects, including noise and pole-zero placement. DSP core design for efficient Mitra-Hirano all-pass filter implementation. ALU core and assembly implementation and verification against fixed-point models for accuracy and efficiency.

Wolfson Microelectronics, Edinburgh — *Design Engineer*

October 2005 - June 2011

Summary: My experience at Wolfson encompassed diverse design roles, focusing on **Verilog RTL implementation, verification, and modeling** using Matlab and Simulink.

Key Achievements:

- **Successfully modeled and implemented** CIC filters and a power-efficient microcoded ALU for the WM8900 project.
- **Pioneered the "Class W" envelope tracking filter**, a power optimization solution for headphone amplifiers that saw widespread adoption across multiple product lines. (e.g., WM1605, WM8993, WM8994, WM8995, WM8915, WM1803).
- **Developed an FLL with low audio jitter**, saving power and area over the PLLs currently in use.
- **Designed and Verified the first DC servo** for precise DC offset correction, improving audio quality, and reducing customers BOM cost.
- **Enhanced design methodologies** including the introduction of Ruby-Verilog, optimizing workflow and saving time.
- **Designed and documented new audio filter chains** for the latest WM codecs, providing critical support for implementation and verification.

EDUCATION

COURSES

MEAD: Delta-Sigma Data Converters (2025)
Online DSP Conference (2024)
Online DSP Conference (2023)
U of Strathclyde:
Control Theory (2022)
Advanced DSP (2022)
Online DSP Conference (2022)
Online DSP Conference (2021)
Technical Writing (2019)
People Piece Management Fundamentals (2018)
Doulos:
SystemVerilog (2018)
Steepest Ascent:
DSP Theory, Architectures & Algorithms (2012)
Esperan (Cadence):
SystemVerilog Verification (2011)
SystemVerilog Designer (2011)
RMU: Core Course (2010)
U of Edinburgh: DSP Processor Architecture (2010)
Mathworks:
Matlab for Signal Processing (2008)
Matlab Fundamentals and Programming Techniques (2008)
Doulos:
Expert Verilog Verification (2007)
Comprehensive Verilog (2007)

Edinburgh University — BEng (Hons) Computer Science & Electrical Engineering Degree

2001 - 2005
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